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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,337	07/28/2003	John McCollum	ACT-368	6310

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EXAMINER
SOWARD, IDA M

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,337	MCCOLLUM, JOHN	
	Examiner	Art Unit	
	Ida M. Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8,9,17,18,26,27,35 and 36* is/are allowed.

6)☒ Claim(s) *1-7,10-16,19-25 and 28-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8-27-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Applicant's amendment filed March 21, 2005.

Drawings

The objection to the drawings has been withdrawn due to the amendment filed.

Claim Objections

The objection to claims 4, 11, 22 and 31 has been withdrawn due to the amendment filed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 and 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (US 6,169,693 B1) in view of Ohsawa (US 2004/0026749 A1).

In regard to claim 1, Chan et al. teach a transistor comprising: a p-type substrate 20; an n-type region 18 disposed over the p-type substrate 20; a p-type region 16 disposed over the n-type region 18; spaced apart source and drain regions 12 & 14

disposed in the p-type region 16 forming a channel 34 therein; a control gate 24 disposed above and insulated from the channel 34; the substrate 20, the n-type region 18 and the p-type region 16 are each biased (Figure 1, columns 3-4, lines 40-67 and 1-15, respectively).

In regard to claims 2 and 4, Chan et al. tech the n-type region 18 being a well region (Figure 1, columns 3-4, lines 40-67 and 1-15, respectively).

In regard to claim 3, Chan et al. teach the p-type region 16 being a well region (Figure 1, columns 3-4, lines 40-67 and 1-15, respectively).

In regard to claim 10, Chan et al. teach a floating-gate transistor comprising: a p-type substrate 20; an n-type region 18 disposed over the p-type substrate 20; a p-type region 16 disposed over the n-type region 18; spaced apart source and drain regions 12 & 14 disposed in the p-type region 16 forming a channel 34 therein; a floating gate 22 disposed above and insulated from the channel 34; the substrate 20, the n-type region 18 and the p-type region 16 are each biased (Figure 1, columns 3-4, lines 40-67 and 1-15, respectively).

In regard to claims 11 and 13, Chan et al. tech the n-type region 18 being a well region (Figure 1, columns 3-4, lines 40-67 and 1-15, respectively).

In regard to claim 12, Chan et al. teach the p-type region 16 being a well region (Figure 1, columns 3-4, lines 40-67 and 1-15, respectively).

In regard to the preamble concerning a transistor “for an integrated circuit”, a preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the

claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See In re Hirao, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and Kropa v. Robie, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987). Also, it would have been obvious to one of ordinary skill that a transistor is for an integrated circuit since it is a well known practice in the art of semiconductor devices.

In regard to the n-type source and drain regions, although the applied references fail to explicitly teach the source and drain regions are n-type, it is within the level of ordinary skill for the source and drain regions to be n-type for it is well known that the polarity or conductivity type of the source and drain is opposite the well or substrate region for proper transistor operation.

However, Chan et al. fail to teach a fully depleted p-type region.

Ohsawa teaches a fully depleted p-type region 13 (Figure 4A, abstract, page 4, paragraph [0083]).

Chan et al. disclose the claimed invention except for a fully depleted p-type region. Ohsawa teaches that it is known to provide a transistor memory structure with a fully depleted p-type region. It would have been obvious to one having ordinary skill in the art at the time the invention was made modify the transistor memory structure as taught by Chan et al. with the transistor memory structure having a fully depleted p-type

region as taught by Ohsawa to secure good characteristics of data holding (page 4, paragraph [0080]).

Claims 5, 7, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (US 6,169,693 B1) and Ohsawa (US 2004/0026749 A1) as applied to claims 1-4 and 10-13 above, and further in view of Chi et al. (6,060,742).

Chan et al. and Ohsawa teach all mentioned in the rejection above. However, Chan et al. and Ohsawa et al. fail to teach an n-type region being a buried layer; and an isolation trench disposed in a p-type region and surrounding source and drain regions, the isolation trench extending into an n-type region.

Chi et al. teach an n-type region 603 being a buried layer; and an isolation trench 605 disposed in a p-type region and surrounding source and drain regions, the isolation trench 605 extending into an n-type region (Figure 6, columns 4-5, lines 43-67 and 1-35, respectively).

Chan et al. and Ohsawa disclose the claimed invention except for an n-type buried layer region and an isolation trench. Chi et al. teach that it is known to provide a transistor memory structure with an n-type buried layer region and an isolation trench. It would have been obvious to one having ordinary skill in the art at the time the invention was made modify the transistor memory structure as taught by Chan et al. and the transistor memory structure having a fully depleted p-type region as taught by Ohsawa combined with the transistor memory structure as taught by Chi et al. having an n-type region being a buried layer to increase the amount of seed electrons injected into the p-

region (columns 2-3, lines 64-67 and 1-2, respectively) and an isolation trench that will result in a preferred smaller spacing (column 5, lines 2-7).

Claims 6 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (US 6,169,693 B1), Ohsawa (US 2004/0026749 A1) and Chi et al. (6,060,742) as applied to claims 5, 7, 14 and 16 above, and further in view of Shinohara et al. (US 2004/0000681 A1).

Chan et al., Ohsawa and Chi et al. teach all mentioned in the rejection above. However, Chan et al., Ohsawa et al. and Chi et al. fail to teach a buried layer laid out in a grid formation.

Shinohara et al. teach a buried layer laid out in a grid formation (Figure 1, page 5, paragraphs [0059]-[0064]).

In regard to the conductivity type of the buried layer, it would have been obvious to one of ordinary skill to interchange conductivity of the region in a transistor as admitted by the Applicant on page 13, paragraph [0035]).

Chan et al., Ohsawa and Chi et al. disclose the claimed invention except for a buried layer region laid out in a grid formation. Shinohara et al. teach that it is known to provide a MOS transistor structure with a buried layer region laid out in a grid formation. It would have been obvious to one having ordinary skill in the art at the time the invention was made modify the MOS transistor structure as taught by Chan et al., the MOS transistor structure having a fully depleted p-type region as taught by Ohsawa and the MOS transistor structure having an n-type region being a buried layer and an

isolation trench as taught by Chi et al. combined with the MOS transistor structure having a buried layer region laid out in a grid formation as taught by Shinohara et al. to prevent short shorting between the source and drain (page 3, paragraph [0022]).

Claims 19-22 and 28-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US 6,329,246 B1) in view of Ohsawa (US 2004/0026749 A1).

In regard to claim 19, Lee teaches a transistor comprising: an n-type substrate 100; an p-type region 102 disposed over the n-type substrate 100; an n-type region 104 disposed over the p-type region 102; spaced apart p-type source and drain regions 106 & 108 disposed in the n-type region 104 forming a channel therein; a control gate 126 disposed above and insulated from the channel; the substrate 100, the p-type region 102 and the n-type region 104 are each biased (Figures 2C and 3, column 3, lines 11-52).

In regard to claims 20 and 22, Lee teaches the p-type region 102 being a well region (Figures 2C and 3, column 3, lines 11-52).

In regard to claim 21, Lee teaches the n-type region 104 being a well region (Figures 2C and 3, column 3, lines 11-52).

In regard to claim 28, Lee teaches a transistor comprising: an n-type substrate 100; an p-type region 102 disposed over the n-type substrate 100; an n-type region 104 disposed over the p-type region 102; spaced apart p-type source and drain regions 106 & 108 disposed in the n-type region 104 forming a channel therein; a floating gate 122 disposed above and insulated from the channel; the substrate 100, the p-type region

102 and the n-type region 104 are each biased (Figures 2C and 3, column 3, lines 11-52).

In regard to claims 29 and 31, Lee teaches the p-type region 102 being a well region (Figures 2C and 3, column 3, lines 11-52).

In regard to claim 30, Lee teaches the n-type region 104 being a well region (Figures 2C and 3, column 3, lines 11-52).

In regard to the preamble concerning a transistor "for an integrated circuit", a preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See In re Hirao, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and Kropa v. Robie, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987). Also, it would have been obvious to one of ordinary skill that a transistor is for an integrated circuit since it is a well known practice in the art of semiconductor devices.

However, Lee fails to teach a fully depleted n-type region.

In regard to the fully depleted "n-type region", it would have been obvious to one of ordinary skill to interchange conductivity of the region in a transistor as admitted by the Applicant on page 13, paragraph [0035]).

Ohsawa teaches a fully depleted region 13 (Figure 4A, page 1, paragraph [0010]).

Lee discloses the claimed invention except for a fully depleted n-type region. Ohsawa teaches that it is known to provide a MOS transistor structure with a fully depleted region. It would have been obvious to one having ordinary skill in the art at the time the invention was made modify the MOS transistor structure as taught by Lee et al. with the MOS transistor structure having a fully depleted region as taught by Ohsawa to suppress leak current in a scale-down (page 4, paragraph [0080]).

Claims 23 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US 6,329,246 B1) and Ohsawa (US 2004/0026749 A1) as applied to claims 19-22 and 28-31 above, and further in view of Wang (US 2004/0065922 A1).

Lee and Ohsawa teach all mentioned in the rejection above. However, Lee and Ohsawa et al. fail to teach an n-type region being a buried layer; and an isolation trench disposed in a p-type region and surrounding source and drain regions, the isolation trench extending into an n-type region.

Wang teaches a p-type region PBL being a buried layer (Figure 2B, pages 3-4, paragraph [0041]).

Lee and Ohsawa disclose the claimed invention except for a p-type buried layer region. Wang teaches that it is known to provide a MOS transistor structure with a p-type buried layer region. It would have been obvious to one having ordinary skill in the art at the time the invention was made modify the MOS transistor structure as taught by

Lee and the MOS transistor structure having a fully depleted p-type region as taught by Ohsawa with the MOS transistor structure having a p-type region being a buried layer as taught by Wang to provide isolation from the n-type substrate (page 1, paragraph [0013]).

Claims 24 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US 6,329,246 B1), Ohsawa (US 2004/0026749 A1) and Wang (US 2004/0065922 A1) as applied to claims 23 and 32 above, and further in view of Shinohara et al. (US 2004/0000681 A1).

Lee, Ohsawa and Wang teach all mentioned in the rejection above. However, Lee, Ohsawa et al. and Wang fail to teach a p-type buried layer laid out in a grid formation.

Shinohara et al. teach a p-type buried layer 105 laid out in a grid formation (Figure 1, page 5, paragraphs [0059]-[0064]).

Lee, Ohsawa and Wang disclose the claimed invention except for a buried layer region laid out in a grid formation. Shinohara et al. teach that it is known to provide a MOS transistor structure with a p-type buried layer region laid out in a grid formation. It would have been obvious to one having ordinary skill in the art at the time the invention was made modify the MOS transistor structure as taught by Lee, the MOS transistor structure having a fully depleted p-type region as taught by Ohsawa and the MOS transistor structure having a p-type region being a buried layer as taught by Wang combined with the MOS transistor structure having a p-type buried layer laid out in a

grid formation as taught by Shinohara et al. to prevent short shorting between the source and drain (page 3, paragraph [0022]).

Claims 25 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US 6,329,246 B1) and Ohsawa (US 2004/0026749 A1) as applied to claims 19-22 and 28-31 above, and further in view of Chi et al. (6,060,742).

Lee and Ohsawa teach all mentioned in the rejection above. However, Lee and Ohsawa et al. fail to teach an isolation trench disposed in an n-type region and surrounding source and drain regions, the isolation trench extending down into a p-type region.

Chi et al. teach an isolation trench 605 disposed in an n-type region N-WELL and surrounding source and drain regions, the isolation trench 605 extending down into a p-type region P-WELL (Figure 6, columns 4-5, lines 43-67 and 1-35, respectively).

Lee and Ohsawa disclose the claimed invention except for an isolation trench. Chi et al. teach that it is known to provide a transistor memory structure an isolation trench. It would have been obvious to one having ordinary skill in the art at the time the invention was made modify the transistor memory structure as taught by Lee and the transistor memory structure having a fully depleted region as taught by Ohsawa with the transistor memory structure having an isolation trench as taught by Chi et al. to provide a transistor that will result in preferred smaller spacing (column 5, lines 2-7).

Allowable Subject Matter

Claims 8-9, 17-18, 26-27 and 35-36 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not disclose, make obvious, or otherwise suggest the structure of the applicant's together with the other limitations of the independent claims. For instance, Shinohara et al. (US 2004/0000681 A1) teach the claimed transistor structure but falls to teach the substrate, p-type region and the p-type buried layers each biased such that the p-type region is fully depleted. Masamichi (JP 61123171 A) teaches each of the n-type buried layers being biased but fails to teach biasing the other regions, a fully depleted region and the claimed transistor structure. Lee (US 6,329,246 B1) teaches biasing the other regions but fails to teach biasing each of the buried layers and a fully depleted region. And Ohsawa (US 2004/0026749 A1) teaches a fully depleted p-type region but fails to teach the claimed biased layers. The dependent claims being further limiting and definite are also allowable.

Response to Arguments

Applicant's arguments filed 03-21-2005 have been fully considered but they are not persuasive.

In regard to the remarks on pages 16-17, paragraphs 3-4 and 1-4, respectively, Chan et al., the primary reference, teach disclose the a substrate 20, an n-type region

18 and a p-type region 34 each being biased Vsub, Vnw and Vpw, respectively as shown in Figure 1. Ohsawa, the secondary reference, for the p-type silicon layer being fully depleted. Since Chan et al. and Ohsawa are both from the same field of endeavor (MOSFET memory structures), the purpose disclosed by Ohsawa would have been recognized in the pertinent art of Chan et al. Also, in regard to a substrate, an n-type region and a p-type region each being biased such that a p-type region is fully depleted, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function, In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

In regard to the remarks concerning Lee on pages 19-20, last and first paragraphs, respectively, Lee, the primary reference, teach discloses the a substrate 100, an n-type region 104 and a p-type region 102 each being biased VN-well, VN-well and VP-well, respectively as shown in Figure 3. And the same as stated above, Ohsawa, the secondary reference, is utilized for the teaching of the p-type silicon layer being fully depleted.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

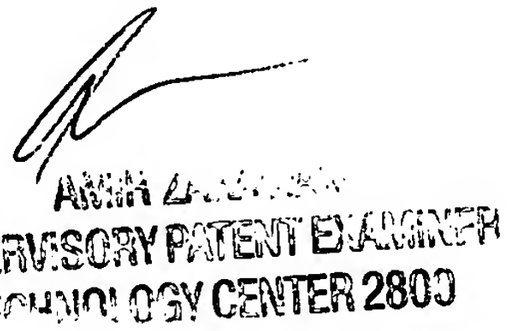
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday, 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
May 26, 2005



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TECHNOLOGY CENTER 2800

Approved 5/26/05 mp

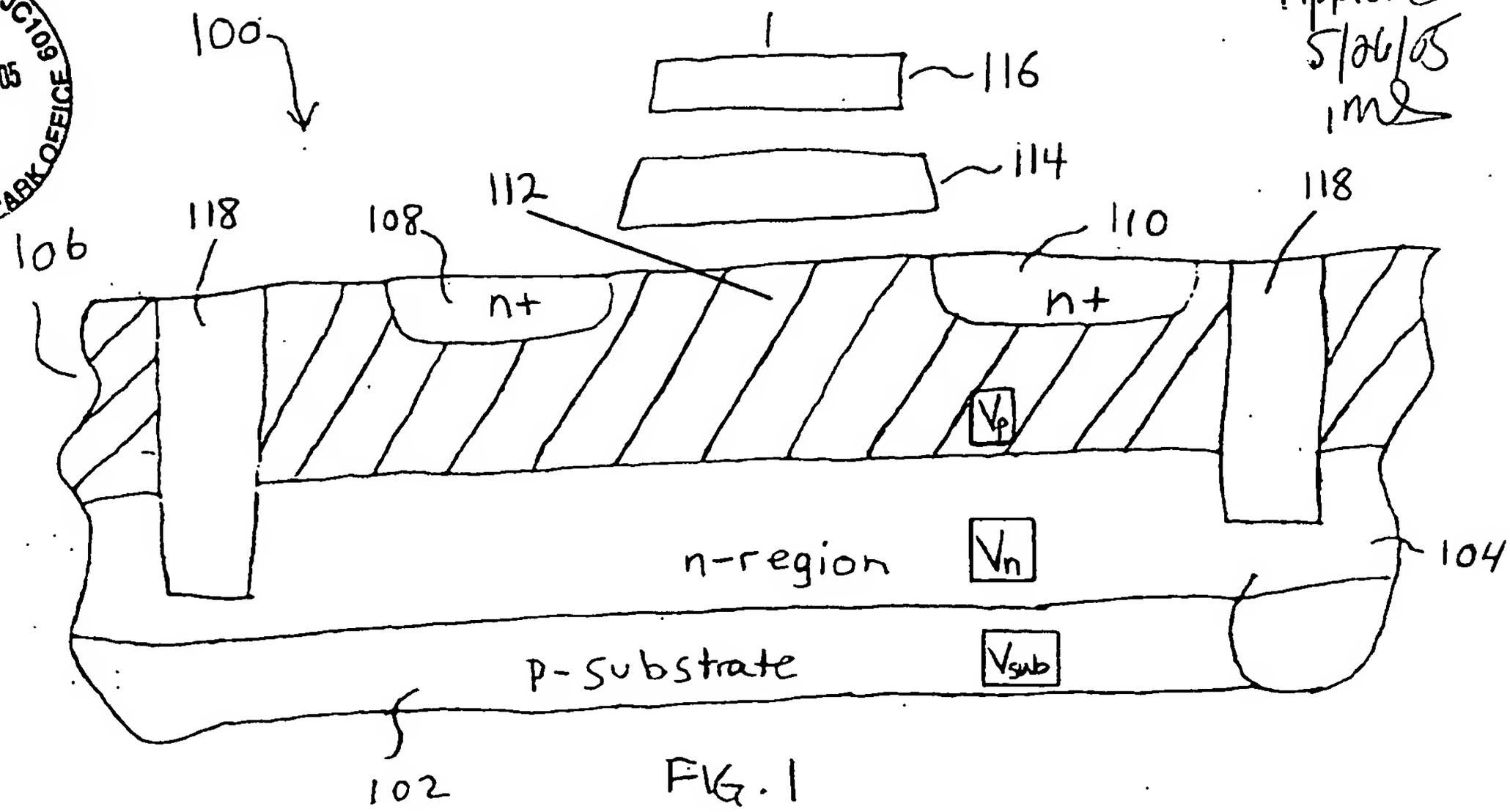

FIG. 1

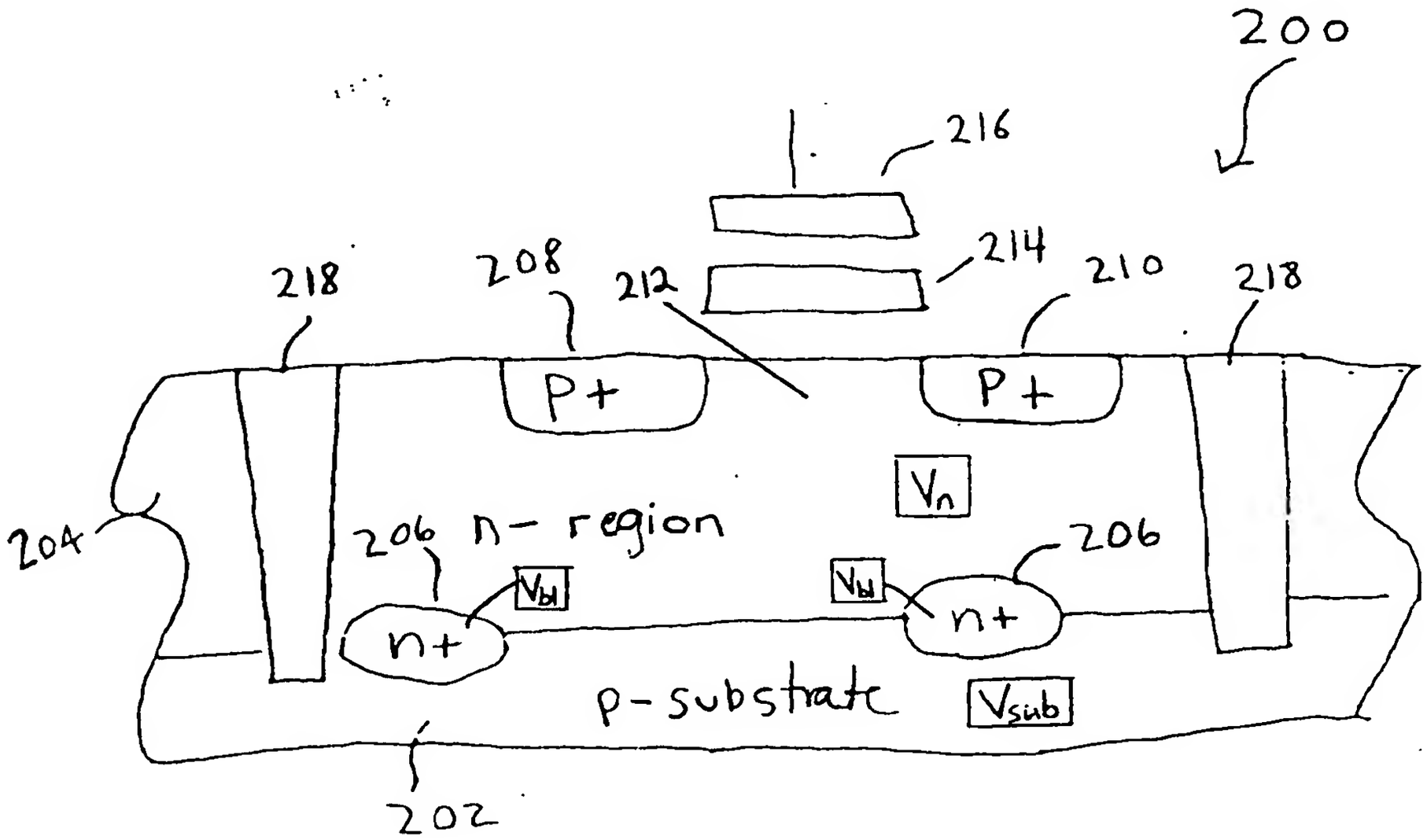

FIG. 3

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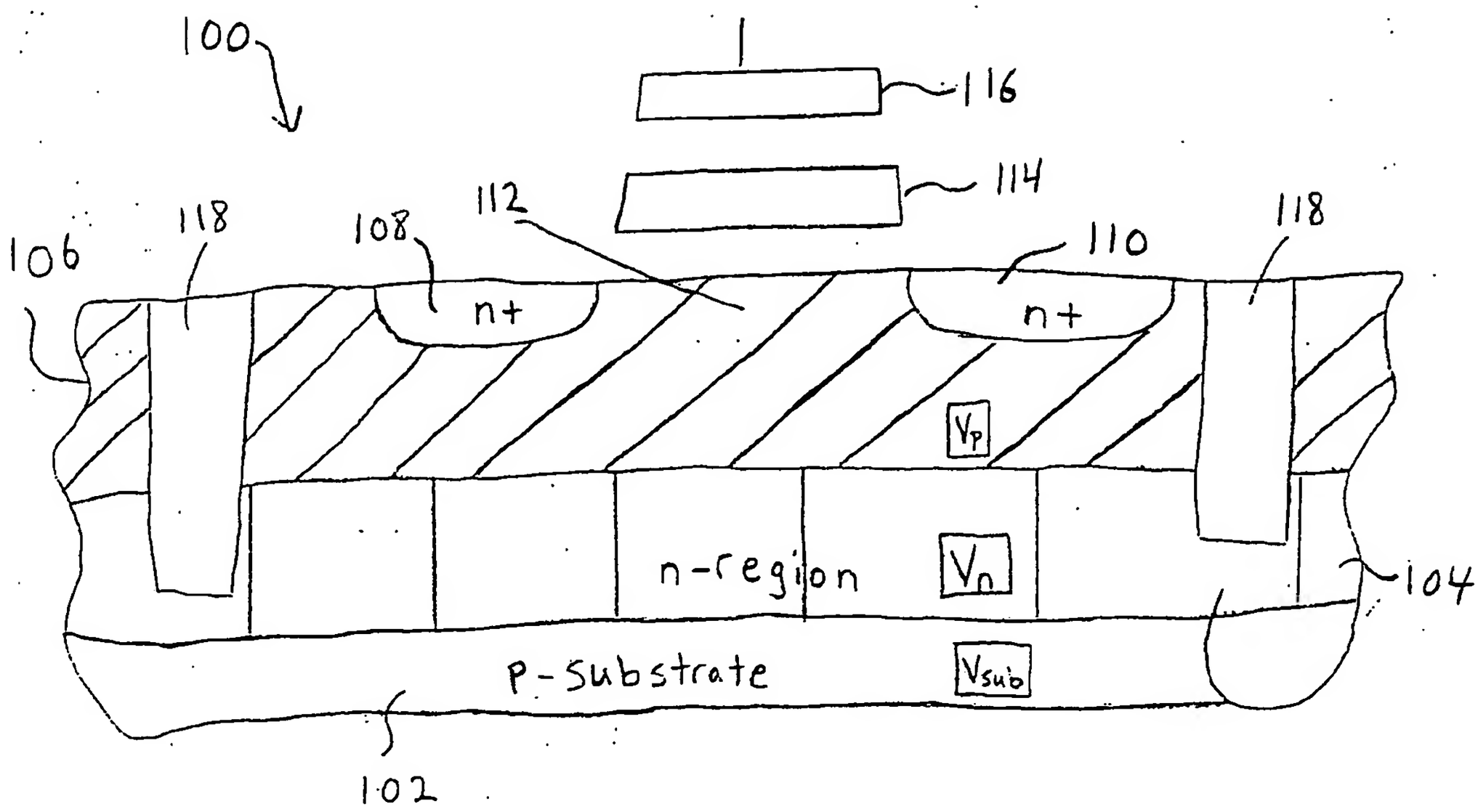

FIG. 4